



## Layered TMDFETS for Nano Devices: A Short Review

Topical Review

Subhra Dhar<sup>\*</sup> and Manisha Pattanaik

Department of Information Technology, VLSI Design,  
ABV - Indian Institute of Information Technology and Management,  
Gwalior 474 015, India

\*Corresponding author: [sdharmos@gmail.com](mailto:sdharmos@gmail.com)

**Abstract.** Two-dimensional semiconducting materials of the *transition-metal-dichalcogenide* (TMD) family, such as MoS<sub>2</sub> and WSe<sub>2</sub>, have been intensively investigated in the past few years, and are considered as workable contenders for next-generation electronic devices. In this very brief review, we provide an evaluation of devices based on monolayer and multi layer two-dimensional materials, outlining their prospects as a technological option for low power transistor designs. Our study revealed that the two dimensional transition-metal-dichalcogenide are versatile materials which may be used as a single layer or multi layered with diverse properties enabling to suit a wide range of low power applications. Further study divulges that experimental investigations of monolayer TMD transistors encourage workers with excellent carrier mobilities required for low power applications, whereas multilayer TMD transistors reveal WS<sub>2</sub> to be an excellent channel material for making of high performance FET required for energy efficient electronic applications. We understand that this work will provide an important step towards the design and performance evaluation of FETs in low power applications based on two-dimensional materials. Further, the results obtained due to the TMDs so far, prove beneficial to both states of FET operation i.e. ON state and OFF state, when compared to conventional materials.

**Keywords.** Monolayer; Multilayer 2D materials; Transition metal dichalcogenides; MoS<sub>2</sub> transistors; Low power

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## 1. Introduction

In the past few decades, layered *transition metal dichalcogenides* (TMDs) materials have been considered in the nanomaterial research community due to their encouraging properties as atomically thin, 2D forms are a comparatively innovative, motivating area for nanotechnology, with many applications in nanoelectronics [1]. Currently, TMDs have captivated significance due to their natural abundance, exceptional and dissimilar properties among the 2D materials [2, Figure 1]. These are layered materials facilitating exfoliation into two-dimensional layers of single unit cell thickness, with strong in-plane bonding and weak out-of-plane interactions. The huge bandgaps noticed in quite a lot of materials of the TMD group make them remarkable channel materials in logic transistors, and the direct bandgaps in several single-layer TMDs open up many avenues in nanoelectronics [1]. Molybdenum disulfide ( $\text{MoS}_2$ ) has been one of the most studied layered TMDs due to widespread in nature as molybdenite. Unlike graphene,  $\text{MoS}_2$  makes it possible to tune the carrier transport in an electronic device, thus enabling various device functions [2]. Its capacity to diminish short channel effects in extremely scaled devices due to chemical inertness, mechanical properties, excellent electrostatic confinement together with its high thermal stability, makes  $\text{MoS}_2$  transistors superior contenders for mixed-signal low power electronics [3]. Researchers have attained state-of-the-art fabrication technology and physics-based model for  $\text{MoS}_2$  *field-effect-transistors* (FETs) to realize large-scale complete *computer-aided design* (CAD) flow [4]. Also,  $\text{MoS}_2$  technology has been developed in order to develop the design of complex systems with device modeling, circuit simulation and parametric cell-based layout circuit development [5].

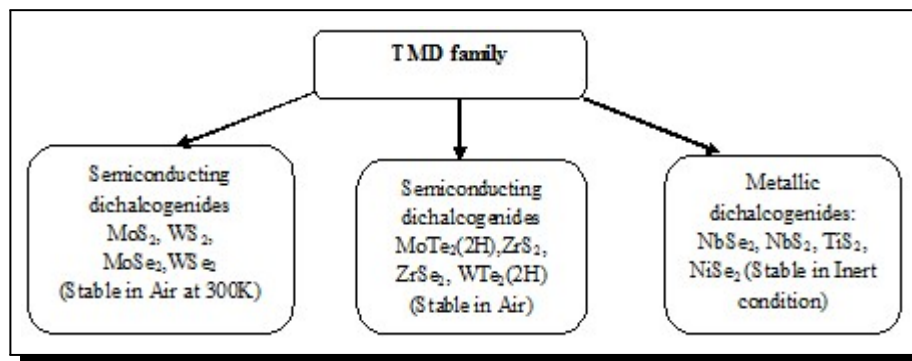


Figure 1. The TMD family [2]

To replace silicon in the next generation nanoelectronic devices,  $\text{MoS}_2$  is being considered as the novel material due to its distinctive set of electrical properties. High mobility of carriers of the order of  $700 \text{ cm}^2/\text{Vs}$ , high drive current, lesser subthreshold swing, higher immunity to short channel effects as compared to silicon, outstanding interface quality with the gate dielectric, high current ON/OFF ratio ( $10^9$ ) with low standby power dissipation, reasonably low ( $\sim 3.3$ ) dielectric constant and enormous tunable bandwidth [6] are few promising properties of  $\text{MoS}_2$ .

TMD monolayers are the thinnest semiconductors possible and offer many advantages for scaling of electronic devices. Monolayer  $\text{MoS}_2$  is comprised of a lone layer of molybdenum atoms

sandwiched between two layers of sulphur atoms for a total thickness of 0.65 Å. Monolayer MoS<sub>2</sub> is a semiconductor with a direct bandgap of 1.8 eV, compensating the limitation of gapless graphene, thus enabling 2D materials to be used in the generation next switching devices [5].

MoS<sub>2</sub>-based transistors, with an intrinsic band gap, offers numerous advantages compared with the graphene transistors, to name a few of them viz., excellent current saturation, large intrinsic gain and higher ON/OFF ratio. Utilizing these exceptional advantages, few-layer or multi layer MoS<sub>2</sub> transistors is an interesting alternative for high-speed low-power electronics and also can be used to construct functional circuits [7]. Mono and multiple layers of MoS<sub>2</sub> have been also investigated as channel materials in FETs for digital as well as analogue applications confirming MoS<sub>2</sub> FETs can achieve both current and power amplification in principle.

This work is a short review on the emergence of layered TMDFETS and the progress made by mono layer as well as multilayer TMDs as a consequence in the field of low power applications in the last few years. The paper is structured as follows. Section 2 describes monolayer TMDFETS and the advances made so far. Section 3 describes multilayer TMDFETS and the progress made so far. Section 4 concludes the paper.

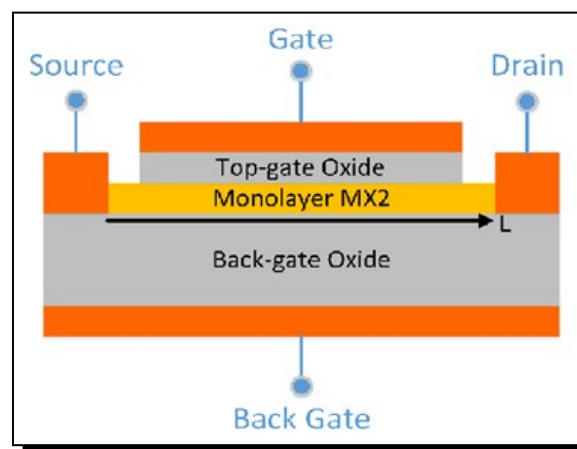
## 2. Monolayer TMDFETS

Power dissipation being a major concern in MOSFETS, various designs of FETs and various materials were proposed in the last two decades to address this issue. In the recent years, it is observed that transistors using 2D materials resulted in better gate control and smaller leakage current. Phosphorene, which is being considered for digital applications is a new 2D p-type high-mobility semiconductor. A monolayer free-standing phosphorene is a semiconductor with a direct band gap of 1.0 eV. Monolayer phosphorene being one atomic layer thick, is more stable and exhibits a lower defect density than TMDs like as MoS<sub>2</sub>. Monolayer phosphorene is bendable and competent of mechanical exfoliation very much like graphene and TMDs, for instance MoS<sub>2</sub>, exhibit greater electrical, optical and mechanical properties than their bulk counterparts [8]. Encouraging ON/OFF current ratio due to single layer phosphorene suitable for low power applications can be observed in Table 1.

Among other mono layered TMDs, WTe<sub>2</sub>-tunneling FETs, though [see Table 1] emerges as the most promising candidate for both *high power* (HP) and *low operation power* (LOP) FETs as mandatory by ITRS 2024, reveals that the decisive scaling stops around 5nm even for the atomically thin materials [9]. HfS<sub>2</sub> is yet another new TMD, which has not been experimentally explored as the material for electron devices [10]. Theoretically, it is found that single-layer HfS<sub>2</sub> has the prospect for well-balanced mobility of 1,800 cm<sup>2</sup>/V·s and bandgap 1.2 eV for a high ON/OFF ratio and consequently can be a good candidate for a low-power devices as is evident from Table 1.

Large-scale single-layer MoS<sub>2</sub> grown by CVD demonstrated excellent characteristics such as record mobility for CVD MoS<sub>2</sub>, record current density, ultra-high ON/OFF current ratio and GHz RF performance for integrated devices and circuits [11]. The ON/OFF current ratio of the device exceeds 10<sup>8</sup>, making these devices perfect for ultra-low power applications such as circuits for flat panel display. Experimental observations have proven that the carrier mobility

in polycrystalline CVD single-layer MoS<sub>2</sub> is 40 cm<sup>2</sup>/V·s and single-crystalline exfoliated multi-layer MoS<sub>2</sub> is 150 cm<sup>2</sup>/V·s and thus permits MoS<sub>2</sub> FETs to operate even at GHz frequency. Experimental results also acknowledged that innovative device concept and design should be used to make the most of the properties of 2D materials in logical devices. From further studies we observed that the current ON/OFF ratio shows a decreasing trend with increasing thickness. The dependence of current ratio on the thickness of TMD and thereby significance of multi layer TMDs arising in context of low power applications is very well investigated in [8]. Further studies show that in the absence of energy barrier at the source or drain terminals, the electrons in this surplus MoS<sub>2</sub> will add significantly to the leakage current. The possible merits of multilayer MoS<sub>2</sub> are, counterbalanced by a high leakage current, leading to a notably reduced current ON/OFF ratio. Therefore, identifying the optimal thickness range is of substantial importance for material synthesis and realistic device applications of the 2D TMDs. It is very well understood that that the atomic scale thickness also is of utmost significance when weighed against materials like silicon as it can lessen short-channel effects. 2D semiconductors like the monolayer TMDs, allow an extremely high level of electrostatic control at the ultimate limit of thickness. In recent work, we come across simulation results confirming monolayer MoS<sub>2</sub> and other similar lone layer TMDs have high resistance to short channel effects due to its small thickness and sustain their high ON/OFF ratio for small channel lengths. It is also reported that measurements on multilayer devices with channel lengths in the sub-100 nm range have confirmed the absence of short-channel effects at this scale. Because of its 2D nature, monolayer MoS<sub>2</sub> is especially responsive to the presence of charges in the charge trapping layer. This results in about 10<sup>4</sup> variation in currents between states in which the memory is stored and erased. 2D semiconductors devices is an imperative step toward the realization of electronics and low stand-by power integrated circuits based on two-dimensional materials as discussed by researchers in [12]. A current ON/OFF ratio between 1 × 10<sup>4</sup> and 1 × 10<sup>7</sup> and a bandgap exceeding 400 meV are desirable for any plausible substitute of silicon in digital logic devices [13]. Furthermore, at high impurity doping densities, MoS<sub>2</sub> FETs are favourable with superior device electrostatics, and higher ON-current for high-performance as well as low-standby-power applications.



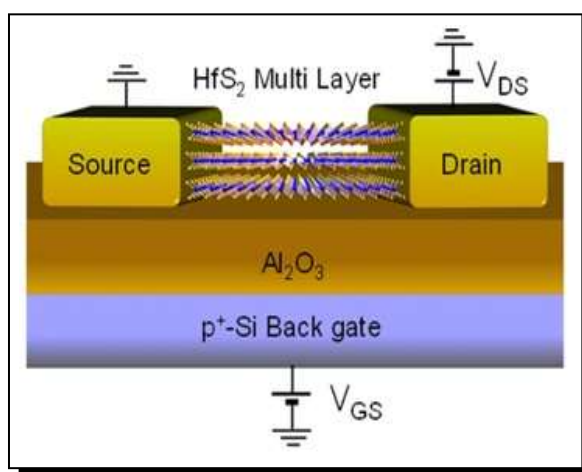
**Figure 2.** Schematic of monolayer TMDFET [14]

### 3. Multilayer TMDFETS

MoS<sub>2</sub>, a typical layered TMD, has a suitable bandgap in the range of 1.3 to 1.8 eV and is thickness-reliant. For monolayers it is of the value 1.8 eV. Consequently, transistors of both mono- and multilayer-MoS<sub>2</sub> films have demonstrated high ratio of ON-state to OFF-state current ( $I_{on}/I_{off} > 10^6$ ) with realistic electron mobility. This makes the layered TMDs highly competent in fields of low-power switches/circuits, nonvolatile memory devices, photodetectors etc. In transistor applications, multilayer MoS<sub>2</sub> with a lesser bandgap is of higher potential than the monolayer counterpart due to its three-times higher density of states and conduct current along several channels resulting in high drive current [15]. Recent works have confirmed that multilayer MoS<sub>2</sub> is appropriate for large area high density electronics. As devices with more thickness reveal higher breakdown current limitations than thinner devices, multilayer MoS<sub>2</sub> FETs are also beneficial when compared to mono-layer devices by carrying additional power at the same time as having the same device footmark. While mobility and current ratios are chief device parameters for logical circuits, the current transportation limit is also significant for applications requiring high current and power.

Utilizing the exclusive properties offered by multilayer MoS<sub>2</sub> transistors, on analysis of device characteristics such as electron mobility and electrical breakdown limit, by focusing on their reliance on device constraints such as MoS<sub>2</sub> thickness, leads to motivating results as studied by workers in [16]. The concept of per layer current was accounted for mono-layer MoS<sub>2</sub> FET, with a superior per-layer current limit of  $1.18 \times 10^6$  Am<sup>-1</sup> than for the multilayer devices  $1.76 \times 10^4$  A m<sup>-1</sup>.

Multilayer devices are more suited for certain circuit applications as they can attain higher mobility and superior current limit than mono-layered MoS<sub>2</sub> FETs. We come across few-layer MoS<sub>2</sub> FETs which were fabricated and these devices showed current ratios greater than  $10^6$ . In multilayer MoS<sub>2</sub> FETs, current saturation which is extremely important for building both digital and analog circuits has been observed for the first time [5]. This property is lacking in most graphene FETs due to its zero bandgap and is also not observed in the monolayer MoS<sub>2</sub> FETs.



**Figure 3.** Schematic of multi layer TMDFET [10]



Experimental investigation of electrical breakdown in multilayer MoS<sub>2</sub> FETs reveals the current ratio  $I_{ON}/I_{OFF}$  to be around  $10^7$ . FETs based on multi-layered *p*-doped WSe<sub>2</sub> indicated that WSe<sub>2</sub> has the possibility to exhibit higher carrier mobilities through the identification of suitable substrates, as well as contact materials [17]. Multilayer WS<sub>2</sub> crystal certainly is an excellent channel material, when compared to other semiconducting TMDs, for the making of high performance FET essential for energy saving in addition to high power electronics applications [18].

For building a useable FET, a key requirement is the ability to turn it off by applying a voltage to the gate electrode. 2D semiconductors are well-suited for this purpose, as the existence of a band gap permits the material to be depleted of charge carriers. For example, it is observed that a high semiconducting band-gap (~1.5 eV and 1.1 eV, respectively) prevents achieving high ON-currents in mono- and bi-layer WSe<sub>2</sub> [19]. This can be seen in Table ?? where the current ratios remain the same for mono- as well as bi-layer WSe<sub>2</sub>. This is also an encouraging implication of the presence of band gaps in TMDFETS over graphene FETs.

Few challenges faced by the layered TMDs are, to arrive at high-performance devices based on two dimensional materials with the conventional lithography processes, as their incompatibility damages the atomic structure and deteriorate the electronic properties. Moreover, it is observed that though various doping techniques have been suggested and attempted, doping of 2D materials with higher efficiency still remains a daunting task. Controlling carrier type, concentration and the Fermi level is one of the essential technology required for the digital logic and analog applications [20]. As high Schottky barriers reduce the drive current and mobility, the device performance gets limited. Further, contact resistance between the metal electrodes and MoS<sub>2</sub>, remains a major challenge in MoS<sub>2</sub>-based transistors that remains to be worked upon.

**Table 1.**  $I_{ON}/I_{OFF}$  ratioS of mono layer TMD - and multi layer TMDs

S. No.	TMDs	Device characteristics	Monolayer TMDFETs	Multilayer TMDFETs
1	MoS <sub>2</sub>	$I_{ON}/I_{OFF}$	$> 10^8$ [12], [13]	$> 10^7$ [5] $> 10^6$ [15] $\sim 10^7$ [16]
2	Phosphorene	$I_{ON}/I_{OFF}$	$\sim 10^5$ [8]	$\sim 10^6$ [22]
3	WTe <sub>2</sub>	$I_{ON}/I_{OFF}$	$\sim 10^5$ [9]	—
4	WSe <sub>2</sub>	$I_{ON}/I_{OFF}$	$> 10^6$ [21]	$> 10^6$ [19]
5	HfS <sub>2</sub>	$I_{ON}/I_{OFF}$	—	$> 10^4$ [10]

## 4. Conclusion

As we reviewed the work done in the area of layered TMDFETs in recent years, we understand that this work will provide an important step towards the design and performance evaluation of FETs in low power applications based on two-dimensional materials. Further, the results

obtained due to the TMDs prove beneficial to both states of FET operation i.e. ON state and OFF state, when compared to conventional materials.

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## Competing Interests

The authors declare that they have no competing interests.

## Authors' Contributions

All the authors contributed significantly in writing this article. The authors read and approved the final manuscript.

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